An AlGaAs/InGaAs Pseudomorphic HEMT Modulator Driver IC with Low Power Dissipation for 10-Gb/s Optical Transmission Systems

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***Abstract*— An optical modulator driver integated circuit (IC) has been developed for 10-Gb/s optical communication systems. To achieve both high-frequency (HF) operation and low power dissipation, 0.2-μm T-shaped gate AlGaAs/InGaAs pseudomorphic high electron-mobility transistors (HEMT's) have been employed for their large transconductance g_m of 610 mS/mm and high cutoff frequency f_T of 67.5 GHz. In addition, optimizing input logic swing, switching transistor size in the output driver, and using cascode-current mirror circuits with small output conductance enable power dissipation as low as 1 W to be achieved at a 10-Gb/s nonreturn-to-zero (NRZ) signal output with 3 $V_{p\text{-}p}$. This is the lowest value ever reported for power dissipation. As an additional function, the output voltage swing can be controlled in the range from 2 to 3.3 $V_{p\text{-}p}$ by the current mirror circuit for the purpose of adjusting the optical-output-signal duty factor through an optical modulator.**

***Index Terms*—High-speed integrated circuits, integrated circuit design, MODFET integrated circuits, optical communication, optical transmitters.**

I. Introduction

FOR 10-Gb/s long-haul optical communication systems, transmission systems with external modulation are preferable to direct modulation in terms of suppressing the broadening of spectral linewidth at high bit-rate modulation. The driver integrated circuit (IC) for an electroabsorption (EA) modulator must normally have both high-speed operation and a large drive voltage to provide the large voltage swing of over 2 $V_{p\text{-}p}$ required to ensure sufficient extinction ratio at 10 Gb/s [1]. There is also a strong demand for driver IC's with low power dissipation to enable the design of an air-cooled system [2]. Several reports describe large-output driver IC's using high electron-mobility transistors (HEMT's), heterojunction bipolar transistors (HBT's), and Si-bipolar transistors [3]–[5]. An HEMT IC can operate on a lower supply voltage than HBT or Si-bipolar IC's, so it has the advantage of low power dissipation. For high-speed operation, an HEMT IC usually consists of source-coupled FET logic (SCFL) circuits. In SCFL circuits, reducing power dissipation lessens the internal logic swing and lowers drain-to-source voltage of the switching transistor. The high-frequency (HF) performance of switching transistors must be improved to give a low power dissipation without degradation of switching speed.

The authors' approach has been to adopt 0.2-μm-gate AlGaAs/InGaAs pseudomorphic HEMT's for the driver IC. The HEMT's have higher transconductance and cutoff frequency than pseudomorphic 2DEG FET's described in [3], so the driver IC can operate with lower power dissipation. In the circuit design process, the relation between the input logic swing and the gatewidth of the switching transistor was derived to obtain an output of over 3 $V_{p\text{-}p}$, thereby optimizing output driver transistor size to make the input logic swing as small as possible. Since current mirror circuits with a cascode configuration are used to provide high impedance current sources, the IC can control the input logic swing using external current sources. These current mirror circuits greatly improve HF performance for single-ended input as well as input logic swing controllability. As a result, the IC is capable of both 3-$V_{p\text{-}p}$ output and 1-W dissipation with a 10-Gb/s nonreturn to zero (NRZ) signal. The IC can also adjust the output voltage swing from 2 to 3 $V_{p\text{-}p}$. This paper describes the device structure, circuit design, and characteristics of the IC.

II. Device

Fig. 1 shows a schematic cross section of the AlGaAs/InGaAs pseudomorphic HEMT. A pH-adjusted citric acid : NH_4OH:H_2O_2 solution [6] is used for gate recessing to

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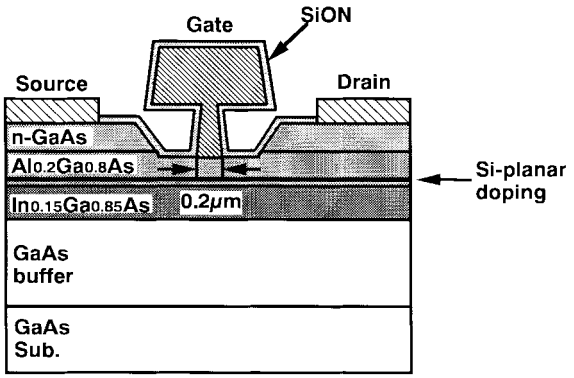


Fig. 1. Schematic cross section of the AlGaAs/InGaAs pseudomorphic HEMT.

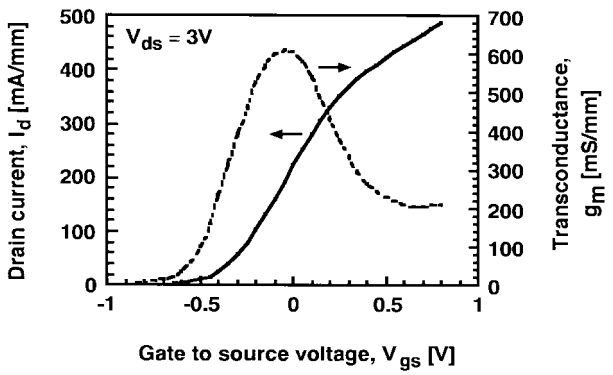


Fig. 2. Drain current and transconductance dependence on gate-to-source voltage of pseudomorphic HEMT.

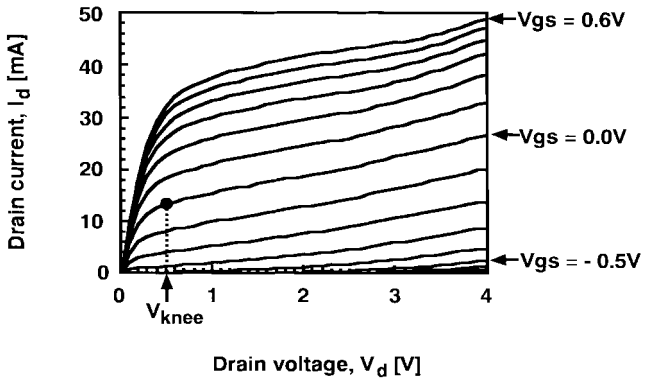


Fig. 3. I–V characteristics of pseudomorphic HEMT.

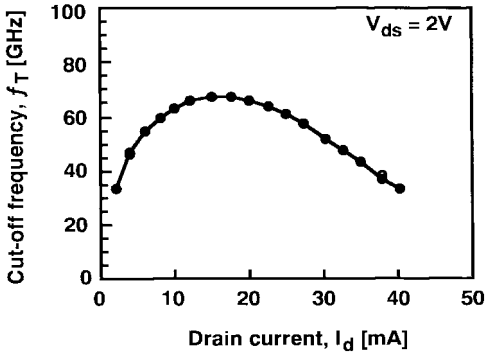


Fig. 4. Measured f_T of pseudomorphic HEMT.

achieve the small deviation of threshold voltage essential to integrated circuits. Fig. 2 shows the dependence of measured drain current I_d and transconductance g_m on gate voltage $V_{\rm gs}$ of the HEMT. When $V_{\rm gs} \approx 0$ V, the maximum g_m is as high as 610 mS/mm. Typical threshold voltage is -0.8 V and the gate-to-drain breakdown voltage $V_{\rm gdo}$ is as high as 10 V. Because of their high electron mobility, HEMT's with low drain-to-source knee voltage $V_{\rm knee}$ are effective for reducing supply voltage [7]. Fig. 3 shows I–V characteristics of the HEMT with 100-μm-gatewidth. When $V_{\rm gs} = 0$ V, $V_{\rm knee}$ is as low as 0.5 V. Fig. 4 shows the characteristics of measured f_T in terms of I_d for the 100-μm gatewidth HEMT. As can be seen, maximum f_T is 67.5 GHz. This result is effective for producing lower power dissipation 10-Gb/s driver IC's.

III. Circuit Design

Fig. 5 shows the circuit diagram for the driver IC. The IC consists of an input buffer with an SCFL (0, -1 V) interface, a two-stage differential amplifier acting as a pre-driver, and an output driver. The first stage of the pre-driver provides single-ended to differential conversion. This paper's circuit design target for output voltage swing was 3 $V_{\rm p\text{-}p}$. This corresponds to a modulation current of 60 $mA_{\rm p\text{-}p}$ in the output driver. Increasing the output voltage swing involves increasing the input logic swing of the output driver. In SCFL circuits, however, the maximum input logic swing is limited by supply voltage and drain-to-source knee voltage because differential switching transistors must operate in the current saturation region for high-speed operation. For the output driver shown in Fig. 6, the high level $V_{\rm high}$ and low level $V_{\rm low}$ of the input logic swing are described by the following formulas:

$$V_{\rm high} \le -(V_{\rm out} + V_{\rm knee}) + V_{\rm gs\_on} \tag{1}$$

$$V_{\rm low} \ge V_{SS} + V_{\rm knee} \tag{2}$$

where $V_{\rm out}$ is the output voltage swing required, $V_{\rm knee}$ is the drain-to-source knee voltage, and $V_{\rm gs\_on}$ is the gate-to-source voltage necessary to make modulation current $I_{\rm MOD}$ flow across external load resistor R_L. The maximum input logic swing $V_{\rm sw\_max}$ obtained by subtracting $V_{\rm low}$ from $V_{\rm high}$ is expressed by

$$\begin{aligned} V_{\rm sw\_max} &= V_{\rm gs\_on} - (V_{\rm out} + V_{SS} + 2 \cdot V_{\rm knee}) \\ &= V_{\rm gs\_on} + 1.2. \end{aligned} \tag{3}$$

For this IC, parameters $V_{\rm out}$, V_{SS}, and $V_{\rm knee}$ are 3.0, -5.2, and 0.5 V. The switching transistors operate in the current saturation region, so $V_{\rm gs\_on}$ is given by

$$V_{\rm gs\_on} = \left(\frac{I_{\rm MOD}}{K_u \cdot W_{\rm sw}}\right)^{1/2} + V_{\rm th} \tag{4}$$

where K_u is the transconductance parameter per-unit gatewidth of 0.68 mA/(V$^2 \cdot \mu$m), $W_{\rm sw}$ is the gatewidth of the switching transistor, and $V_{\rm th}$ is the threshold voltage of -0.8 V. From (3) and (4), $V_{\rm sw\_max}$ for $W_{\rm sw}$ can be expressed

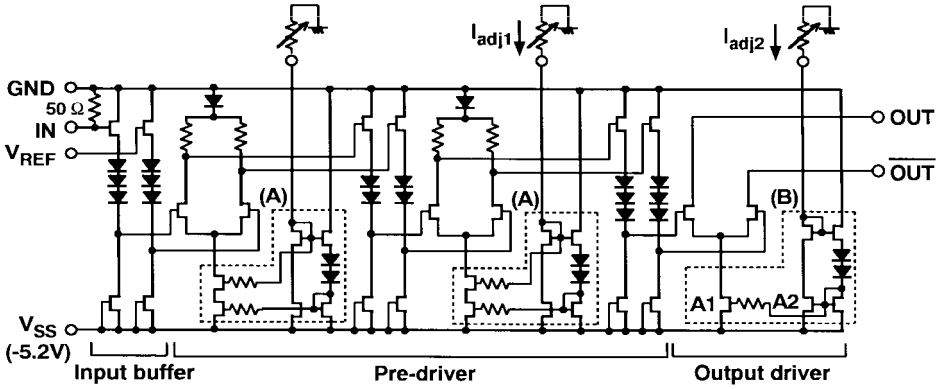


Fig. 5. Circuit diagram for driver IC.

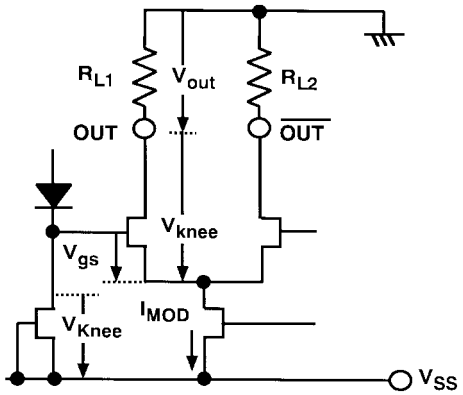


Fig. 6. Driver circuit diagram for determining the maximum input voltage swing.

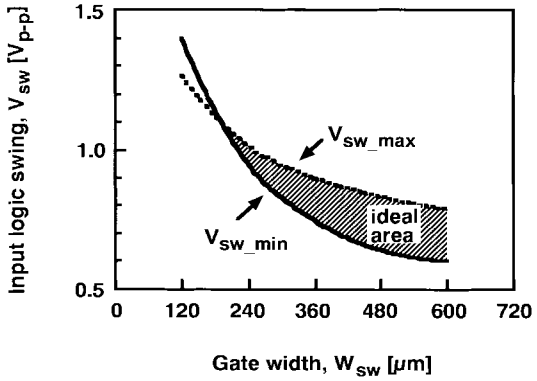


Fig. 7. Minimum and maximum input logic swing against the gatewidth of the switching HEMT.

as follows:

$$V_{\mathrm{sw\_max}} = \left(\frac{I_{\mathrm{MOD}}}{K_u \cdot W_{\mathrm{sw}}}\right)^{1/2} + V_{\mathrm{th}} + 1.2 \approx \left(\frac{90}{W_{\mathrm{sw}}}\right)^{1/2} + 0.4. \quad (5)$$

In Fig. 7, $V_{\mathrm{sw\_min}}$ and $V_{\mathrm{sw\_max}}$ are plotted against W_{sw}, where $V_{\mathrm{sw\_min}}$ (shown by a solid line) is the simulated input logic swing necessary for achieving output voltage swing of 3 $V_{\mathrm{p\text{-}p}}$ at least, and $V_{\mathrm{sw\_max}}$ (shown by a dotted line) is estimated by (5). In the simulation of the output driver, the authors' considered that the parasitic capacitance connected in parallel with a 50-Ω load resistor, which includes on-chip metallization-line capacitance and the pad capacitance, was 0.3 pF. In this design, both V_{sw} and W_{sw} are optimized within the ideal area shown by oblique lines in Fig. 7, because the output voltage swing is smaller than 3 $V_{\mathrm{p\text{-}p}}$ under the condition of V_{sw} below $V_{\mathrm{sw\_min}}$ and the switching speed is not improved under the condition of V_{sw} above $V_{\mathrm{sw\_max}}$. For the switching speed, the relation between V_{sw} and W_{sw} shown in Fig. 8 is also important [8]. Rise time at the output terminal of the output driver t_r decreases as the input logic swing increases, and this decrease is larger as W_{sw} becomes smaller. From Fig. 8, one can see that a W_{sw} of 360 μm can give the fastest t_r for a lower input logic swing. In this paper, a W_{sw} of 360 μm and a V_{sw} of 0.8 $V_{\mathrm{p\text{-}p}}$ were determined in consideration of the switching speed and the relation shown in Fig. 7.

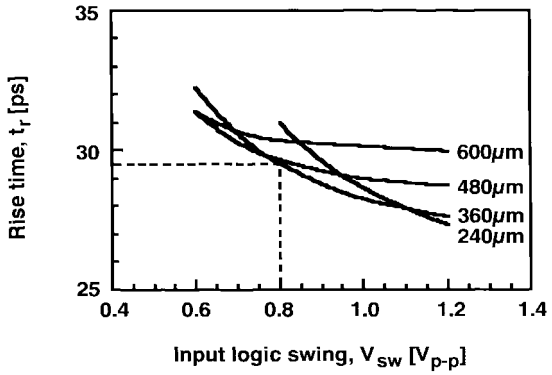


Fig. 8. Rise time at output terminal dependence on the input logic swing.

Because W_{sw} and V_{sw} also influence power dissipation of the IC P_d, the authors discuss the relation between both P_d and W_{sw}, and P_d and V_{sw}. The increase in W_{sw} involves the increase in the parasitic capacitance loaded for the pre-driver. The decrease in t_r increases the currents flowing through the source followers of the pre-driver as well as input logic swing, indicating that the P_d is deeply related to the driverbility of the pre-driver, which makes t_r fast. In Fig. 9, the P_d for different W_{sw} was simulated, where the currents flowing through the source followers and V_{sw} were optimized so that t_r keeps 30 ps. Over a W_{sw} of 480 μm, the P_d is rapidly increased. The V_{sw} also depends on the P_d. The P_d as a function of V_{sw} is shown in Fig. 10. In this

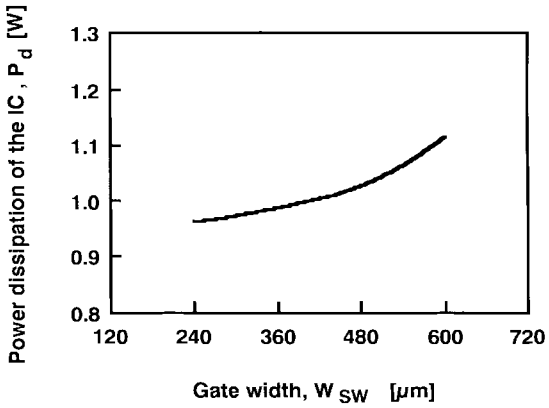


Fig. 9. Power dissipation of the IC for the different gatewidth of the switching transistor.

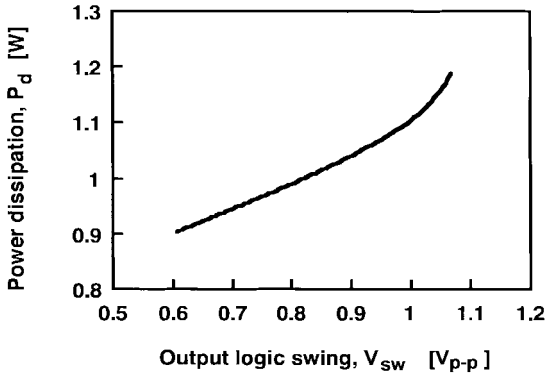


Fig. 10. Power dissipation of the IC as a function of the output logic swing of the pre-driver.

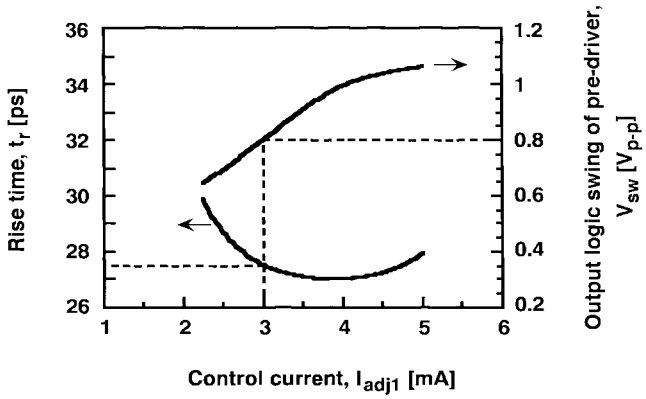


Fig. 11. Rise time at output terminal of the output driver and the output logic swing of pre-driver dependence on the control current I_{adj1}.

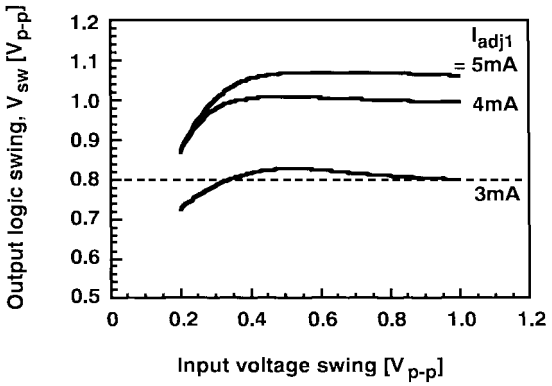


Fig. 12. The output logic swing of pre-driver dependence on the input voltage swing of the IC for different control current I_{adj1}.

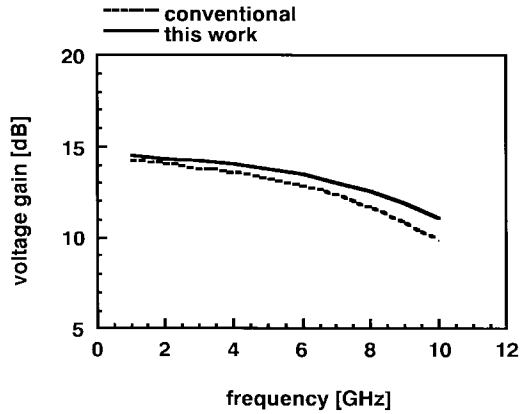


Fig. 13. Frequency response of the pre-driver.

simulation, the V_{sw} is increased by the currents dissipated in the differential pair transistors of the pre-driver because the increase in load resistance degrades frequency response of the pre-driver. Fig. 10 shows P_d increases as V_{sw} increases. Thus, it is essential that both W_{sw} and V_{sw} are optimized as small as possible for reducing P_d. The W_{sw} of 360 μm and V_{sw} of 0.8 $\mathrm{V_{p\text{-}p}}$ utilized in this paper are sufficiently small to reduce P_d.

To obtain both the high-speed and large voltage output characteristics, the output logic swing of the pre-driver needs to be precisely controlled. A current mirror circuit (A) with a cascode configuration is adopted as the current source for each differential stage of the pre-driver. This reduces changes in the internal logic swing due to supply voltage variations. The output logic swing of the pre-driver is adjusted by external current source I_{adj1} as shown in Fig. 11. When $I_{\mathrm{adj1}} = 3$ mA, the output logic swing is 0.8 $\mathrm{V_{p\text{-}p}}$, leading to a t_r of 27.5 ps. As can be seen from Fig. 12, a pre-driver with a high gain of 14 dB keeps the output logic swing constant over a change in the single input signal from 0.4 to 1 $\mathrm{V_{p\text{-}p}}$.

Another merit of using the current mirror circuit (A) will now be mentioned. The voltage gain of the pre-driver is very affected by the output conductance of the current sources since the pre-driver operates with single-ended input. In Fig. 13, the simulated voltage gain of the pre-driver in the IC is compared with that of conventional circuit such as the current mirror circuit (B). Because the output conductance of the current source in this paper is very small, in spite of large drain conductance of the HEMT, the loss of the voltage gain is extremely small. The SPICE transient analysis shows that the difference of the voltage gain shown in this paper and a conventional circuit corresponds to the difference of the output voltage swing of 0.1 $\mathrm{V_{p\text{-}p}}$ at pre-driver output. As expected from Figs. 7 and 8, the decrease in the output voltage swing causes degradation of rise time or output voltage swing at the output terminal of the IC. This degradation in the conventional circuit leads to the increase of P_d, even though it would be compensated by an increase in the internal logic swing. In

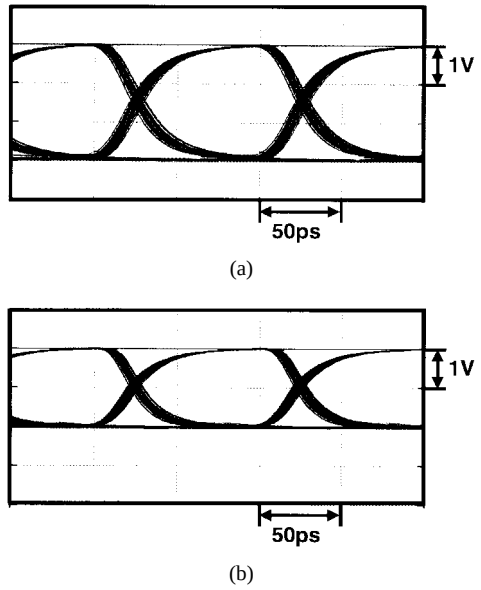


Fig. 14. Simulated output diagram at 10-Gb/s, $2^7 - 1$ PRBS for different control currents I_{adj2}. (a) $I_{\mathrm{adj2}} = 3.5$ mA and (b) $I_{\mathrm{adj2}} = 2.0$ mA.

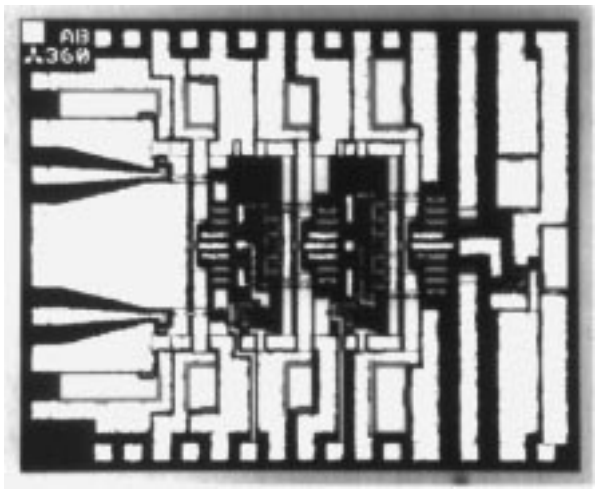


Fig. 15. Microphotograph of driver IC.

this paper's circuit, utilization of the current mirror circuit (A) saves the P_d of about 50 mW as shown in Fig. 10.

The output driver also includes a current mirror circuit (B). The output voltage swing is controlled by the current mirror circuit in order to adjust the duty factor of the optical output signal through an optical modulator, which has nonlinear characteristics for optical power versus input voltage. The ratio of gatewidth of A_1 to A_2 is set at 16:1 to make control current I_{adj2} small. Another merit of utilizing a current mirror circuit is that output voltage variations according to supply voltage or ambient temperature can be compensated for using an external bias control circuit [9]. Fig. 14 shows output simulations for different values of the control current I_{adj2} at 10 Gb/s. The 1-$V_{\mathrm{p\text{-}p}}$ input signal is a pseudo-random bit sequence (PRBS) of $2^7 - 1$. When $I_{\mathrm{adj2}} = 3.5$ mA, the output voltage swing is 3 $V_{\mathrm{p\text{-}p}}$. The minimum output voltage swing is 2 $V_{\mathrm{p\text{-}p}}$ when $I_{\mathrm{adj2}} = 2.0$ mA.

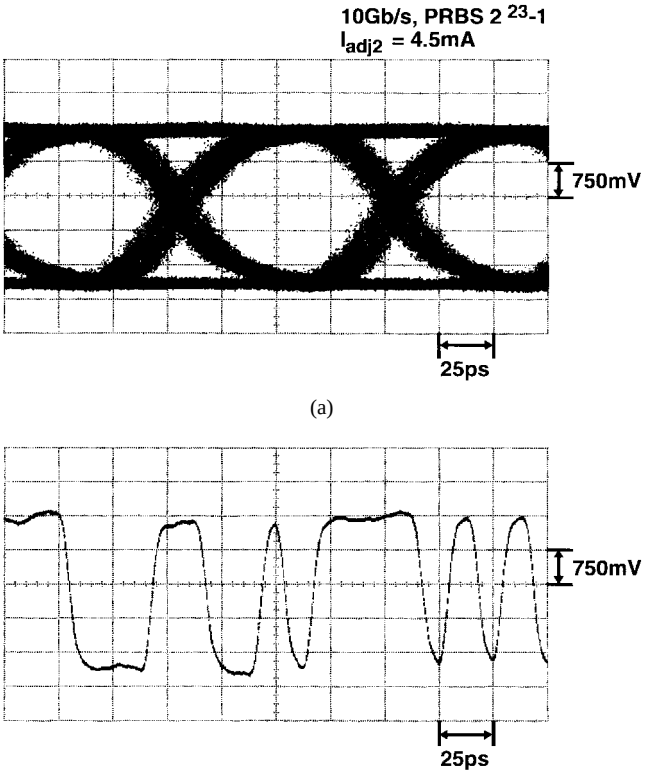
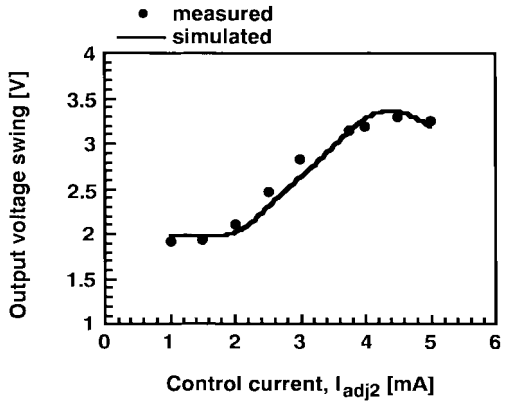


Fig. 16. (a) Measured output diagram and (b) section of the output pulse sequence for output voltage swing of 3.3 $V_{\mathrm{p\text{-}p}}$ at 10 Gb/s.

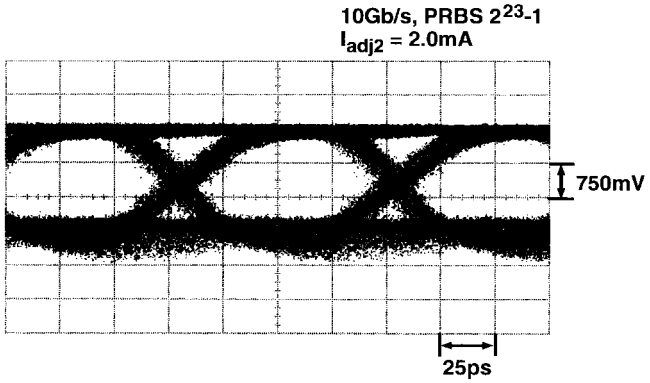
Fig. 15 is a microphotograph of the driver IC. A coplanar structure with 50-Ω impedance is employed for the input and output lines. Both IN and V_{REF} terminals can be terminated to ground by on-chip 50-Ω resistors to allow differential input. Metal–insulator–metal capacitors are integrated as bypass capacitors to stabilize the power supplies at −5.2 V. Chip size is 3.0 mm × 2.5 mm.

IV. Characteristics

The IC was assembled on a ceramic carrier and measured in 50-Ω testing systems. Fig. 16 shows the output diagram and a section of the output pulse sequence for SCFL input with PRBS of $2^{23} - 1$ when the IC is driving a 50-Ω load. The maximum voltage swing of 3.3 $V_{\mathrm{p\text{-}p}}$ and rise/fall times (20%–80%) of 32.4/30.2 ps are obtained at 10 Gb/s. Good eye opening is observed and sensitivity for the input voltage swing in single-input operation is as low as 0.4 $V_{\mathrm{p\text{-}p}}$. Fig. 17 shows the measured and simulated output voltage swing dependence on the control current I_{adj2} shown in Fig. 5, and the output diagram for the minimum output voltage swing when $I_{\mathrm{adj2}} = 2.0$ mA. The output diagram is well opened and has no edge-steepness degradation. The output voltage swing changes from 2 to 3 $V_{\mathrm{p\text{-}p}}$ in proportion to I_{adj2}, a range which is more than sufficiently wide for adjusting the duty factor of the optical output signal through an optical modulator. Measurements agree well with the simulations. The power dissipation for 3 $V_{\mathrm{p\text{-}p}}$ output voltage swing is 1.0 W, the lowest value ever reported [2]–[4].



(a)



(b)

Fig. 17. Measured and simulated output voltage swing dependence on the control current (a) I_{adj2} and the output diagram at (b) I_{adj2} of 2.0 mA.

V. Conclusion

A modulator driver IC using 0.2-μm-gate AlGaAs/InGaAs HEMT's has been developed for 10-Gb/s optical transmission systems. Despite the large output voltage swing of 3 $V_{p\text{-}p}$, the IC has power dissipation of only 1 W. The driver IC will contribute to the construction of 10-Gb/s long-haul optical communication systems.

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